

**REMARKS**

Claims 1-4, 6-11, 51-55, 56-60 and 62-66 are pending in the application. Withdrawn claims 5, 12-50, 56 and 61 have been cancelled. Claim 60 has been cancelled. Claims 1, 3, 6, 10, 51-55, and 57 have been amended. New claims 62-66 have been added. No new matter has been introduced.

Claim 51 stands rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent 6,037,577 to Tanaka et al. ("Tanaka"). The rejection is respectfully traversed.

Claim 51 recites, *inter alia*, "an input lead for receiving at least one readout signal from a pixel array comprising at least a background signal; [and]...a readout element connected to provide a readout signal from the first capacitive element when the switching element is switched off and from the first and second capacitive elements when the switching element is switched on, wherein the combined signal is a signal to be subtracted from an image signal."

The invention of claim 51 relates to a circuit having first and second capacitive elements which are connected by a switching element. The claimed memory circuit receives at least one signal, a background signal from a pixel array and stores the charge in a first capacitive element. A signal is generated by combining signals from the first and second capacitive elements, via a conductive path. The generated signal is subtracted from the image signal. Tanaka relates to amplifying an image output for a pickup device. Tanaka does not teach a circuit for storing a background signal and generating a signal to be subtracted from the image signal. Accordingly, Tanaka fails to teach "an input lead for receiving at least one readout signal from a pixel array

comprising at least a background signal; [and]...a readout element connected to provide a readout signal from the first capacitive element when the switching element is switched off and from the first and second capacitive elements when the switching element is switched on, wherein the combined signal is a signal to be subtracted from an image signal,” as recited in independent claim 51. Applicant respectfully requests withdrawal of the rejection.

Claims 1, 4, 52, 55, 57 and 60 stand rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent 6,747,695 to Afghahi (“Afghahi”). The rejection is respectfully traversed.

Independent claim 1 recites, *inter alia*, “a pixel array circuit that outputs an image signal including a background signal caused by at least one of non-uniformity of illumination and optical shading; [and] a memory array circuit, coupled to said pixel array circuit, to store the background signal.”

Independent claim 52 recites, *inter alia*, “a pixel array circuit for outputting an image signal including a background only signal; [and] a memory array circuit, coupled to said pixel array circuit, for receiving and storing the background only signal.”

Independent claim 57 recites, *inter alia*, “a pixel array circuit, formed in said substrate, for providing an image signal and a background signal caused by at least one of non-uniformity of illumination and optical shading; [and] a memory array circuit, formed in said substrate, coupled to said pixel array circuit, each memory element in said memory array corresponds to a pixel circuit in said pixel array circuit, for storing the background signal.”

The invention of claims 1, 52, 57 and 60 relate to an integrated circuit, imaging system and an imaging device each having a memory array circuit and a data subtraction circuit. The data subtraction circuit removes an undesirable background signal from the image signal. The background signal can be caused by, for example, non-uniformity of illumination and optical shading of the optics which results in unwanted shading patterns in the image signal. Specification at [0002]. In addition, the memory circuit contains a memory for storing the background data. Afghahi relates to an integrated CMOS imager in which the pixel signals are processed to compensate for dark current noise produced within the semiconductor substrate. Afghahi fails to even mention a pixel signal having a background signal caused by at least one of non-uniformity of illumination and optical shading much less subtracting the background signal of the image from the image signal. Further, Afghahi teaches away from a memory device for storing noise or background signals. *See* Afghahi at col. 1, lines 55-67. Afghahi instead teaches compensation for dark voltages without the need for extra storage. *Id.*

Accordingly, Afghahi fails to teach “a pixel array circuit that outputs an image signal including a background signal caused by at least one of non-uniformity of illumination and optical shading; [and] a memory array circuit, coupled to said pixel array circuit, to store the background signal,” as recited in independent claim 1; “a pixel array circuit for outputting an image signal including a background only signal; [and] a memory array circuit, coupled to said pixel array circuit, for receiving and storing the background only signal,” as recited in independent claim 52; and “a pixel array circuit, formed in said substrate, for providing an image signal and a background signal caused by at least one of non-uniformity of illumination and optical shading; [and] a memory array circuit, formed in said substrate, coupled to said pixel array circuit, each memory

element in said memory array corresponds to a pixel circuit in said pixel array circuit, for storing the background signal,” as recited in independent claim 57.

Claim 55 depends from independent claim 52 and is allowable for at least the reasons discussed above and claim 4 depends from independent claim 1 is allowable for at least the reasons discussed above. Claim 60 has been cancelled. Accordingly, Applicant respectfully requests withdrawal of the rejection.

Claims 2-3, 6-11, 53-54 and 58-59 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Afghahi in view of U.S. Patent 5,734,152 to Goren et al. (“Goren”). The rejection is respectfully traversed.

Independent claim 6 recites, “[a] method for processing analog image data in an imager chip, said method comprising the steps of: receiving analog image data, said analog image data including a background signal, caused by at least one of non-uniformity of illumination and optical shading, and a temporal signal; performing a subtraction operation to separate the background signal from the temporal signal; and performing an enhancement operation on the temporal signal to generate an edge-enhanced signal.”

Claim 6 relates to a method for processing image data having a background signal. An undesirable background signal of the image signal is removed from the temporal signal. The background signal can be caused by non-uniformity of illumination and optical shading of the optics which results in unwanted shading patterns in the image signal. Specification at [0002].

Afghahi relates to an integrated CMOS imager in which the pixel signals are processed to compensate for dark current noise of the image sensor produced within the semiconductor substrate. Afghahi does not discuss a pixel signal having a background component much less subtracting the

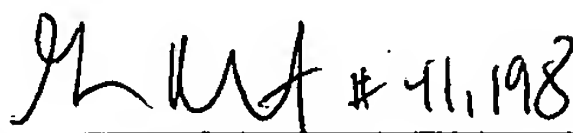
background signal of the image from the temporal signal. Goren relates to optical scanners and processors for the same and specifically describes an enhancement filter. However, Goren fails to discuss a pixel signal having a background signal much less subtracting the background signal from the temporal signal. Accordingly, Afghahi and Goren, whether considered alone or in combination, fail to teach “[a] method for processing analog image data in an imager chip, said method comprising the steps of: receiving image data, said analog image data including a background signal, caused by at least one of non-uniformity of illumination and optical shading, and a temporal signal; performing a subtraction operation to separate the background signal from the temporal signal; and performing an enhancement operation on the temporal signal to generate an edge-enhanced signal,” as recited in independent claim 6. Accordingly, Applicant respectfully requests withdrawal of the rejection.

Claims 2-3, 53-53 and 58-59 respectfully depend from independent claims 1, 52 and 57 and are allowable for at least the reasons discussed above with respect to independent claims 1, 52 and 57. Accordingly, Applicant respectfully requests withdrawal of the rejection.

In view of the above, Applicant believes the pending application is in condition for allowance. Favorable action on the merits is earnestly solicited.

Dated: January 4, 2008

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